ABSTRACT OF THE DISCLOSURE

A memory storage system includes a line cache including a plurality of pages. A first central processing unit (CPU) accesses data stored in the pages of the line cache. A first memory device stores data that is loaded into the line cache when a miss occurs. After an initial miss, the line cache prevents additional misses as long as the first CPU is addressing sequential memory locations of the first memory device. When the miss occurs, n pages of the line cache are loaded with data from sequential locations in the first memory device, wherein n is greater than one. When the CPU requests data from an m^{th} page of the n pages in the line cache, wherein m is greater than one and less than or equal to n, the line cache loads p additional pages with data from sequential locations in the first memory device.